REMARKS

Claim Rejections

Claims 25-28, 33-34, 36, and 39 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Giri et al. (U.S. 6,765,152) in view of Fjelstad et al. (U.S. 6,573,609). Claims 29-30 and 35 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Giri et al. and Fjelstad et al. in view of Klein et al. (U.S. 2004/0145051). Claim 31 is rejected under 35 U.S.C. §103(a) as being unpatentable over Giri et al. and Fjelstad et al. in view of Kikuma et al. (U.S. 6,621,169). Claim 32 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Giri et al. and Fjelstad et al. in view of Koopmans (U.S. 2004/0035840). Claims 38 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Giri et al. and Fjelstad et al. in view of Higgins III (U.S. 5,583,377).

Claim Amendments

By this Amendment, Applicant has amended claim 25 of this application to recite a flip chip package including, *inter alai*, a dummy die having an exposed surface located on a bottom thereof, the exposed surface having a metal thermal-conducting layer directly formed thereon to substantially cover the exposed surface located on the bottom of the dummy die, ***the metal thermal conducting layer being electrically isolated from the redistribution layer***. It is believed that the amended claims specifically set forth each element of Applicant's invention in full compliance with 35 U.S.C. § 112. For example, Fig. 4 clearly shows a lack of electrical connections between the metal thermal conducting layer 233 and the redistribution layer 231. In other words, the metal thermal conducting layer 233 is **not** a circuitized layer. *See, also*, p. 6, ll. 9-12. Applicant further submits that the amended claims define subject matter that is patentably distinguishable over the cited prior art, taken individually or in combination.

In the present invention, a dummy die 230, having no electrically calculating function, includes a bottom surface having a high thermal-conducting metal layer 233 configured to dissipate heat from the chip package. Since the high thermal-conducting metal layer 233 is configured to ***conduct heat and not electricity***, the metal layer 233 is electrically isolated from the overlying

redistribution layer 231. It is also important to note that, in order to maximize heat dissipation, this metal layer 233 is directly formed on the bottom of the dummy die to substantially cover the exposed surface located on the bottom of the dummy die. In addition, in one preferred embodiment, the high thermal-conducting metal layer is ***formed by sputtering***, a method specifically selected by Applicant to enhance heat dissipation.

The primary reference to Giri et al. discloses a multi-chip module having chips on two sides including a frame (12), a large semiconductor device (22) located above the thin-film structure, a thin-film structure (18), and a plurality of semiconductor devices (20) located below the thin-film structure. As admitted on p. 3 of the outstanding Office Action, Giri et al. does not disclose a "dummy die have a metal thermal-conducting layer directly formed thereon."

It follows that Giri et al. do not teach or suggest a flip chip package including a dummy die having an exposed surface located on a bottom thereof, the exposed surface having a metal thermal-conducting layer directly formed thereon to substantially cover the exposed surface located on the bottom of the dummy die, the metal thermal conducting layer being electrically isolated from the redistribution layer. Giri et al. also do not teach or suggest a spluttered metal layer on the bottom surface of a dummy die.

The secondary reference to Fjelstad et al. teaches in Fig. 9C and Fig. 4 a connection component including a second metal layer 940b (cited by the Examiner as teaching Applicant's "metal thermal-conducting layer"). It is important to note that this metal layer 940b is clearly shown as electrically connected to conductive vias 945 and planar leads 230. As a result, the metal layer 940b is clearly ***not*** electrically isolated from overlying structures. For example, Col. 21, ll. 57-59 of Fjelstad et al. clearly teaches that the second metal layer 940b of Fig. 9C **is circuitized** so that **a plurality of planar leads 230 are formed** as seen in Fig. 4. Furthermore, with regard to motivation, the skilled artisan would clearly not be motivated to completely defeat the function of the metal layer 940b (to transmit an electrical signal), and use the metal layer 940b as a non-electrical, thermal conducting layer. Nor does the reference suggest such a modification. Applicant also notes that the reference teaches (Col. 14, ll. 22-23, Col. 21, ll. 43-44) that the first interposer 210 is a rigid dielectric material,

such as alumina, etc. Applicant further notes that, as shown in Fig. 9C, separating the first interposer 210 from the metal layer 940b with the second interposer 220 would further diminish any heat conducting function of the first interposer 210 and, thus, warpage would not be substantially reduced.

Fjelstad et al. do not teach or suggest a flip chip package including a dummy die having an exposed surface located on a bottom thereof, the exposed surface having a metal thermal-conducting layer directly formed thereon to substantially cover the exposed surface located on the bottom of the dummy die, the metal thermal conducting layer being electrically isolated from the redistribution layer. Fjelstad et al. also do not teach or suggest a spluttered metal layer on the bottom surface of a dummy die.

On p. 4 of the outstanding Office Action, the Examiner has admitted that Giri and Fjelstad do not disclose "the metal thermal-conducting layer to be a sputtered metal layer...." The Examiner then argues that "sputtered" is a process limitation that Applicant has not shown imparts structural limitations. In response, Applicant notes that Applicant has selected sputtering to form a molecular structure which is particularly suited to heat dissipation (as compared with CVD, ALD, etc). Furthermore, the skilled artisan would clearly understand that a sputtered metal layer yields a certain type of structure having certain depth ranges, formed from certain precursors, and produces a structure having the molecular features of a metal layer which is sputtered (e.g., relatively thick, with high thermal conductivity). As a result, Applicant respectively submits that the Examiner, by not providing teaches from the art disclosing or suggesting each and every feature recited in Applicant's claims, has not shown the requisite *prima facie* case of obviousness with regard to claim 39.

Neither Klein et al., Kikuma et al., Koopmans, nor Higgins III provide the above-noted deficiencies of Giri et al. or Fjelstad et al. Furthermore, Applicant maintains the characterizations and arguments in the Amendment of August 2, 2006 with respect to Klein et al., Kikuma et al., Koopmans, and Higgins III Applicant further submits that even if the teachings of Giri et al., Fjelstad et al., Klein et al., Kikuma et al., Koopmans, and Higgins III were combined, as suggested by the Examiner, the resultant combination does not suggest: a flip chip package including a dummy die having an exposed surface located on a

bottom thereof, the exposed surface having a metal thermal-conducting layer directly formed thereon to substantially cover the exposed surface located on the bottom of the dummy die, the metal thermal conducting layer being electrically isolated from the redistribution layer; nor does the combination suggest a spluttered metal layer on the bottom surface of a dummy die.

Applicant submits that there is not the slightest suggestion in either Giri et al., Fjelstad et al., Klein et al., Kikuma et al., Koopmans, or Higgins III that their respective teachings may be combined as suggested by the Examiner. Case law is clear that, absent any such teaching or suggestion in the prior art, such a combination cannot be made under 35 U.S.C. § 103. Applicant further maintains that neither Giri et al., Fjelstad et al., Klein et al., Koopmans, nor Higgins III disclose, or suggest a modification of their specifically disclosed structures that would lead one having ordinary skill in the art to arrive at Applicant's claimed structure. Applicant hereby respectfully submits that no combination of the cited prior art renders obvious Applicant's amended claims.

Summary

In view of the foregoing amendments and remarks, Applicant submits that this application is now in condition for allowance and such action is respectfully requested. Should any points remain in issue, which the Examiner feels could best be resolved by either a personal or a telephone interview, it is urged that Applicant's local attorney be contacted at the exchange listed below.

Respectfully submitted,

Date: March 14, 2007 By: 

Demian K. Jackson
Reg. No. 57,551

TROXELL LAW OFFICE PLLC
5205 Leesburg Pike, Suite 1404
Falls Church, Virginia 22041
Telephone: 703 575-2711
Telefax: 703 575-2707

CUSTOMER NUMBER: 40144